GOVT. POLYTECHNIC, HAMIRPUR (H.P.)
Lesson Planning and Coverage

Branch: Computer Engineering **Semester: 3rd**

Subject: Computer System Architecture **Session**: August 2024

Teacher: Mukesh Bhardwaj **Laboratory**: Yes

Sr. No.	No of Lectures	Chapter/ Unit Description	Detailed contents	Reference Resources	Remarks
1	04	Introduction	Functional units of Digital Computer,Computer Organization.Computer Design, Computer Architecture, Von-Neumann and Harvard architecture,Bus Interconnection, Evolution of Microprocessors, Concept of Microcomputer,Microcontroller and Embedded Systems.	R1, R2	
2	10	Overview of Digital Electronics	Number systems: Decimal, Binary, Octal and Hexadecimal. Conversion from one number system to other number System, Signed Binary Numbers: Sign Magnitude Representation, One's Compliment Representation and Two's Compliment Representation. Binary Arithmetic: Addition, Subtraction, Binary Arithmetic using one's and Two's Compliment. Fixed and Floating Point Numbers, Computer Codes: BCD, EBCDIC, ASCII. Multiplication Algorithms - Hardware Implementation for Signed-Magnitude Data, Booth Multiplication Algorithm.	R1, R2	
3	10	Digital Logic	Logic Gates: Symbols and Truth Table, Boolean Algebra, Logic Diagram, De Morgan's Theorem, Combinational Circuits: Block Diagram, Half Adder, Full Adder, Flip Flop: SR, D Flip Flop and J K Flip Flop, Example of a sequential circuit, Decoder & Encoder: 3 to 8, Multiplexer & De Multiplexer: 4 to 1 line.	R1, R2	

4	8	Basic Architecture of Microprocessor 8085	Basic features of 8085 Microprocessor, Block Diagram of 8085 Microprocessor, Functions of Various blocks, Concept of Buses, Bus Multiplexing and De-multiplexing, Status Flags, Addressing Modes and Interrupts.	R1, R2	
5	8	Central Processing Unit	Major Components of CPU, General Register Organization, Control Word, Stack Organization-Register and Memory Stack. Reverse Polish Notation and Evaluation of Arithmetic Expressions; Instruction formats – Three Address Instructions, Two Address Instructions, One Address Instructions, Zero Address Instructions. Brief Introduction to RISC and CISC Processors, Concept of Parallel Processing and Pipelining	R1, R2	
6	8	Memory Organisation	Components of memory hierarchy: main memory, auxiliary memory and cache memory,Introduction to Associative Memory, Cache Memory – Locality of Reference, Hit Ratio, Writing into Cache – Write Through, Write Back, Input-Output Interface –Purpose, I/O Versus Memory Bus, Isolated versus Memory-Mapped I/O.	R1, R2	

References:

R1:Computer System Architecture by M. Morris Mano, Pearson Education.
R2:Fundamentals of Microprocessors and Microcontroller by B. Ram, Dhanpat Rai Publications

COURSE OUTCOMES:

After completing this course students will be able to:

CO-1 Understand the basic building blocks of computer system.

CO-2 Design combinational and sequential circuits.

CO-3 Understand the basic architecture and programming of a microprocessor (8085).

CO-4 Demonstrate an understanding of the design of the functional units of a digital computer system.

CO-5 Explain memory hierarchy of a computer system.

Mukesh 01/08/2024

Signature of Teacher with Date

Mukesh Bhardwaj

Signature of HOD