GOVT. POLYTECHNIC, HAMIRPUR (H.P.)
Practical Planning

Branch: Computer Engineering **Semester: 3rd**

Subject: Computer System Architecture **Session**: August 2024

Teacher: Mukesh Bhardwaj **Laboratory**: Yes

Sr. No.	No of Practical hours planned	Aim of the Practical	Reference for Procedure/ Writeup	Remarks
1	2	To study AND, OR, NOT logic gates and verify their truth tables .	R1, R2	
2	2	To study NAND, NOR, Ex-OR logic gates and verify their truth tables.	R1, R2	
3	4	To realize basic gates (AND, OR, NOT) using NAND gates only.	R1, R2	
4	2	To realize basic gates (AND, OR, NOT) using NOR gates only	R1, R2	
5	2	To realize DeMorgan's theorem.	R1, R2	
6	2	To design and implement Half adder &Full adder circuit.	R1, R2	
7	2	To design 7-segment decoder driver.	R1, R2	
8	4	To Verify the truth table of S-R and JK flip flops.	R1, R2	
9	2	To design and implement encoder and decoder.	R1, R2	
10	4	Addition and subtraction of two 8 bit numbers.	R1, R2	
11	2	To add two 8-bit numbers resulting in 16 bits sum.	R1, R2	
12	2	To find largest among two numbers.	R1, R2	
13	2	To sort a list of numbers.	R1, R2	

References:

R1: Computer System Architecture, by M. Morris Mano.

R2: Structured Computer Organization, Andrew S. Tanenbaum. Pearson.

Mukesh
01/08/2024
Signature of Teacher with Date
(Mukesh Bhardwaj)

Signature of HOD